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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,789	08/06/2001	Takahiro Hattori	01FN024US	7380

466 7590 03/17/2004

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,789	HATTORI, TAKAHIRO	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1- 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

A substitute specification explaining a meaning of the claims is required pursuant to 37 CFR 1.125(a) because the Specification text appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors. Following are examples.

Page 16, lines 21 – 25: "At this time, the switch 1 becomes the OFF state once as when the power supply is in the ON state, and is changed from the OFF state to the ON state by performing the slow start operation again". It is not clear, how the power supply can be in either in the ON or OFF state.

Page 15, lines 6 –9: "and in case that the abnormal current such as the short-circuit mode is generated, the composition that the switch 1 is cut off must be taken". Meaning of the underlined phrase is not clear.

A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and (c).

Objection

Claim 6 is objected due to a following phrase, which is hardly understandable: "said gate controlling circuit sets said field effect transistor to the OFF state and

changes said gate voltage again if the purport that the overcurrent is detected is notified by said overcurrent detecting circuit'. Appropriate correction is required.

Claim 7 is objected due to a following phrase: "if it is receives notification". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 6, 7 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). A meaning of the term "purport" in claims 6, 7 and 12 is unclear, because the term was not found in Dictionaries. The term is indefinite because the specification does not clearly redefine the term. For purpose of examination the term was interpreted as "a port of the controller".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 6 - 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by LT1640 Data Sheet from Linear Technology Corp. Regarding Claim 1, the LT 1640 Data Sheet discloses all the elements of the Claim including a switch device having: a field effect transistor connected between an input and an output (element Q1 on page 1); an overcurrent detecting circuit (elements R1, R7, C3, inputs SENSE and Vee in Fig. 8, page 9), which detects an overcurrent when a current flowing in said field effect transistor exceeds a predetermined value; and a gate controlling circuit (output GATE in Fig. 8, page 9, col. 1 and 2, page 9), which controls an ON/OFF state of said field effect transistor by controlling a gate voltage of said field effect transistor. It further discloses that the gate controlling circuit changing the gate voltage such that ON resistance of the field effect transistor is gradually decreased after it rises once when said field effect transistor is changed from the OFF state to the ON state. An evidence for that is a gradual change of the voltage at NODE 2 in automatic restart after current fault shown in Fig. 9, page 10.

Regarding Claim 2, the LT 1640 Data Sheet discloses the gate controlling circuit (Logic and Gate Drive block on page 5) supplied with a control signal from the outside (UV signal on page 5) indicating the OFF state of said field effect transistor and an

overcurrent detecting signal (signals Vee and SENSE on page 5) outputted from the overcurrent detecting circuit (elements R1, R7 and C3 in Fig. 8, page 9).

Regarding Claim 4, the LT 1640 Data Sheet discloses the gate controlling circuit, which sets the field effect transistor to the OFF state in case that the overcurrent detecting circuit detects the overcurrent while the ON resistance of the field effect transistor is gradually decreased. The Fig. 7 and 9 plots and text on pages 9 and 10 demonstrate such case.

Regarding Claim 6, the LT 1640 Data Sheet discloses the gate controlling circuit outputting an active slow start signal to the transistor gate and (through capacitor C1 in Fig. 6a) to overcurrent detecting circuit (resistor R1 in Fig. 6a) while the gate voltage is gradually changing and the FET is in switching process from the OFF state to the ON state. It further discloses the overcurrent detecting circuit, which notifies a port of controller (LOGIC AND DRIVE block in Fig. 6a) that the overcurrent is detected and indirectly (by switching the FET to its OFF state and thus increasing a voltage drop across the FET to above a Vpg threshold) causing a change in the PWRGD signal value (col. 1 and 2, page 4). This signal is sent to outside equipment as indication that the output voltage of controller can be used. Therefore all structural and function limitations of Claim 6 are satisfied.

Regarding Claim 7, the LT 1640 Data Sheet discloses switching OFF the FET, whenever the overcurrent is detected (see Fig. 6b, 7 and 9).

Regarding Claim 8, the LT 1640 Data Sheet discloses a load, which is inherently connected to the output (output of VICOR VI-J3D-CY element in Fig. 6a,page 7) and a smoothing condenser connected to the load in parallel (element C5 in Fig. 6a,page 7).

Regarding Claim 11, the LT 1640 Data Sheet discloses the switch device as a high side switch, since the switch (element Q1 in Fig. 6a) is connected directly to the power supply, rather than to the ground terminal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of Ohshima (US 6,369,556). As was stated above, LT 1640 Data Sheet discloses all elements of Claim 1. However, regarding Claim 3, it does not disclose the gate controlling circuit not holding the switch in the OFF state when the overcurrent due to an inrush current is detected. Ohshima discloses the gate controlling circuit (Fig. 6, col. 15, line 20 – col. 16, line 7), which does not hold the switch in the OFF state even though the overcurrent detecting circuit detects the overcurrent due to an inrush current. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Liner Technology LT 1640

solution by adding the inrush current mask circuit according to Ohshima, because as Ohshima states (col. 15, lines 25 – 38), suppressing the current flow during the inrush state causes undesirable delays in response of the load.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of Chen et al. (US 5,861,775). Claim 5 differs from Claim 1 rejected accordingly by its limitation of a digital to analog converter connected to the gate of the transistor. LT 1640 Data Sheet does not explicitly disclose presence of the analog to digital converter. Chen et al. disclose controlling the high-side switch (element 30 in Fig. 3) by logic level control signals generated by motor controller (element 25 in Fig. 3). The signals undergo the digital to analog conversion in the hi-side driver, which is the level shifter (col. 5, lines 6 – 31). Examiner takes an Official Notice that most of the MOSFET devices require for their switching the gate voltages ranging either from 0 to 2 V, or from 0 to 5V with respect to the source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Linear Technology solution by using the analog to digital converter in a form of the voltage level shifter, because the high-side switch of the LT 1640 (transistor Q1 in Fig. 6a) operating at voltages close to – 48V requires for its switching the gate voltages ranging between – 48 and – 43V (or –48V and – 46 V) with respect to the ground. Therefore, a digital signal produced by the logic block (LOGIC and GATE DRIVE block on page 5), which usually does not exceed range of 5V (with respect to the ground) requires the digital to analog conversion, i.e. level shifting.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of A. Sedra et al., Microelectronic Circuits textbook. Claim 3 differs from Claim 1 rejected accordingly by its limitation of P-channel FET, while the LT 1640 Data Sheet discloses use of N-channel FET. The Sedra et al. textbook discloses both p-channel and N-channel transistors (pages 342 – 345) and shows that they differ only by their polarity and are mutually interchangeable with minor circuit adjustment. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Linear Technology solution by replacing the N-channel FET by P-channel FET, because as well known in the art, the P-channel and N-channel FET's are used according to the voltage polarity. Selection of particular type of FET for given voltage polarity is a routine engineering task.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of A. Sedra et al., Microelectronic Circuits textbook and further in a view of Chen et al. Claim 10 differs from Claim 9 rejected accordingly by its limitation of a digital to analog converter connected to the gate of the transistor. LT 1640 Data Sheet does not explicitly disclose presence of the analog to digital converter. Chen et al. disclose controlling the high-side switch (element 30 in Fig. 3) by logic level control signals generated by motor controller (element 25 in Fig. 3). The signals undergo the digital to analog conversion in the hi-side driver, which is the level shifter (col. 5, lines 6 – 31). Examiner takes an Official Notice that most of the MOSFET devices require for

their switching the gate voltages ranging either from 0 to 2 V, or from 0 to 5V with respect to the source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Linear Technology solution by using the analog to digital converter in a form of the voltage level shifter, because the high-side switch of the LT 1640 (transistor Q1 in Fig. 6a) operating at voltages close to – 48V requires for its switching the gate voltages ranging between – 48 and – 43V (or – 48V and – 46 V) with respect to the ground. Therefore, a digital signal produced by the logic block (LOGIC and GATE DRIVE block on page 5), which usually does not exceed range of 5V (with respect to the ground) requires the digital to analog conversion, i.e. level shifting.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of A. Sedra et al., Microelectronic Circuits textbook and further in a view of Chen et al. Claim 10 differs from Claim 9 rejected accordingly by its limitation of a digital to analog converter connected to the gate of the transistor. LT 1640 Data Sheet does not explicitly disclose presence of the analog to digital converter. Chen et al. disclose controlling the high-side switch (element 30 in Fig. 3) by logic level control signals generated by motor controller (element 25 in Fig. 3). The signals undergo the digital to analog conversion in the hi-side driver, which is the level shifter (col. 5, lines 6 – 31). Examiner takes an Official Notice that most of the MOSFET devices require for their switching the gate voltages ranging either from 0 to 2 V, or from 0 to 5V with respect to the source. Therefore, it would have been obvious to one of ordinary skill in

the art at the time the invention was made to have modified the Linear Technology solution by using the analog to digital converter in a form of the voltage level shifter, because the high-side switch of the LT 1640 (transistor Q1 in Fig. 6a) operating at voltages close to – 48V requires for its switching the gate voltages ranging between – 48 and – 43V (or – 48V and – 46 V) with respect to the ground. Therefore, a digital signal produced by the logic block (LOGIC and GATE DRIVE block on page 5), which usually does not exceed range of 5V (with respect to the ground) requires the digital to analog conversion, i.e. level shifting.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over LT 1640 Data Sheet in a view of Chen et al. (US 5,861,775). Regarding Claim 12, the LT 1640 Data Sheet discloses following elements of the claim including an overcurrent detecting circuit (elements R1, R7, C3, inputs SENSE and Vee in Fig. 8, page 9), which detects an overcurrent when a current flowing in said field effect transistor exceeds a predetermined value; a gate controlling circuit (output GATE in Fig. 8, page 9, col. 1 and 2, page 9), which controls an ON/OFF state of said field effect transistor by controlling a gate voltage of said field effect transistor. . It further discloses that the gate controlling circuit changing the gate voltage such that ON resistance of the field effect transistor is gradually decreased after it rises once when said field effect transistor is changed from the OFF state to the ON state. An evidence for that is a gradual change of the voltage at NODE 2 in automatic restart after current fault shown in Fig. 9, page 10.

It further discloses the gate controlling circuit outputting an active slow start signal to the transistor gate and (through capacitor C1 in Fig. 6a) to overcurrent detecting circuit (resistor R1 in Fig. 6a) while the gate voltage is gradually changing and the FET is in switching process from the OFF state to the ON state. It further discloses the overcurrent detecting circuit, which notifies a port of controller (LOGIC AND DRIVE block in Fig. 6a) that the overcurrent is detected and indirectly (by switching the FET to its OFF state and thus increasing a voltage drop across the FET to above a Vpg threshold) causing a change in the PWRGD signal value (col. 1 and 2, page 4). This signal is sent to outside equipment as indication that the output voltage of controller can be used. Therefore all structural and function limitations of Claim 6 are satisfied.

Additionally, the LT 1640 Data Sheet discloses switching OFF the FET, whenever the overcurrent is detected (see Fig. 6b, 7 and 9).

However, LT 1640 Data Sheet does not explicitly disclose presence of the analog to digital converter. Chen et al. disclose controlling the high-side switch (element 30 in Fig. 3) by logic level control signals generated by motor controller (element 25 in Fig. 3). The signals undergo the digital to analog conversion in the hi-side driver, which is the level shifter (col. 5, lines 6 – 31). Examiner takes an Official Notice that most of the MOSFET devices require for their switching the gate voltages ranging either from 0 to 2 V, or from 0 to 5V with respect to the source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Linear Technology solution by using the analog to digital converter in a form of the voltage level shifter, because the high-side switch of the LT 1640 (transistor Q1 in Fig.

6a) operating at voltages close to – 48V requires for its switching the gate voltages ranging between – 48 and – 43V (or –48V and – 46 V) with respect to the ground. Therefore, a digital signal produced by the logic block (LOGIC and GATE DRIVE block on page 5), which usually does not exceed range of 5V (with respect to the ground) requires the digital to analog conversion, i.e. level shifting.

Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,222,355, US 6,594,129, US 5,530,302.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
02/29/2004

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER